PTFA212001E
PTFA212001F

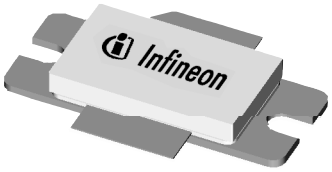
green Product

Thermally-Enhanced High Power RF LDMOS FETs
200 W, 2110 – 2170 MHz

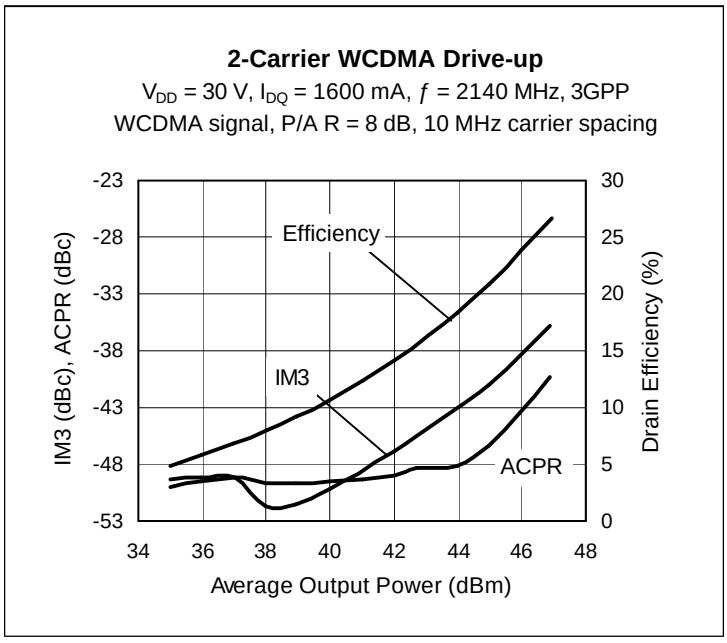
Description

The PTFA212001E and PTFA212001F are 200-watt LDMOS FETs designed for single- and two-carrier WCDMA power amplifier applications in the 2110 to 2170 MHz band. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA212001E
Package H-36260-2



PTFA212001F
Package H-37260-2



Features

- Thermally-enhanced packages, Pb-free and RoHS compliant
- Broadband internal matching
- Typical two-carrier WCDMA performance at 2140 MHz, 30 V
  - Average output power = 50 W
  - Linear Gain = 15.8 dB
  - Efficiency = 28%
  - Intermodulation distortion = –35.5 dBc
  - Adjacent channel power = –40 dBc
- Typical single-carrier WCDMA performance at 2140 MHz, 30 V, 3GPP signal, P/AR = 7.5 dB
  - Average output power = 70 W
  - Linear Gain = 15.5 dB
  - Efficiency = 34%
  - Adjacent channel power = –37 dBc
- Typical CW performance, 2170 MHz, 30 V
  - Output power at P–1dB = 220 W
  - Efficiency = 54%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 5:1 VSWR @ 30 V, 200 W (CW) output power

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics

WCDMA Measurements (tested in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 50 W average
f_1 = 2135 MHz, f_2 = 2145 MHz, 3GPP signal, channel bandwidth = 3.84 MHz , peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15.3	15.8	—	dB
Drain Efficiency	η_D	26.5	28	—	%
Intermodulation Distortion	IMD	—	–35.5	–34	dBc

Two-tone Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 200 W PEP, f = 2140 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	15.8	—	dB
Drain Efficiency	η_D	—	38.5	—	%
Intermodulation Distortion	IMD	—	–28	—	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 30 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.05	—	Ω
Operating Gate Voltage	V_{DS} = 30 V, I_{DQ} = 1.6 A	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	625	W
Above 25°C derate by		3.57	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 200 W CW)	$R_{\theta JC}$	0.28	°C/W

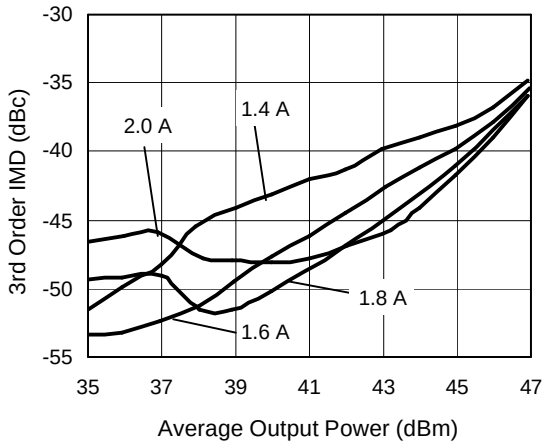
Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA212001E V4	H-36260-2	Thermally-enhanced slotted flange, single-ended	PTFA212001E
PTFA212001F V4	H-37260-2	Thermally-enhanced earless flange, single-ended	PTFA212001F

Typical Performance (data taken in a production test fixture)

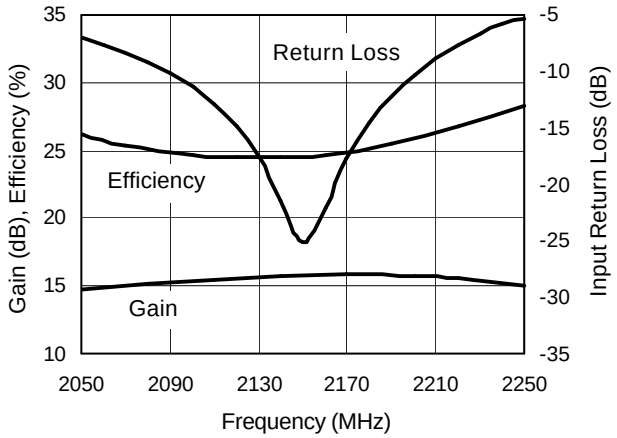
Two-carrier WCDMA at Selected Biases

V_{DD} = 30 V, f = 2140 MHz, 3GPP WCDMA signal,
P/AR = 8 dB, 10 MHz carrier spacing, series show I_{DQ}



Broadband Performance

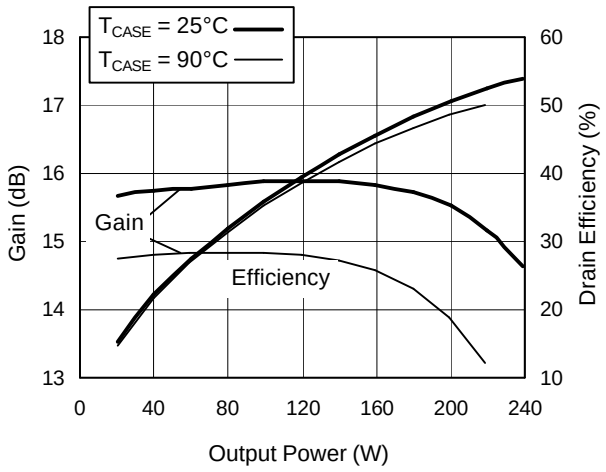
V_{DD} = 30 V, I_{DQ} = 1600 mA, P_{OUT} = 50.0 dBm



Typical Performance (cont.)

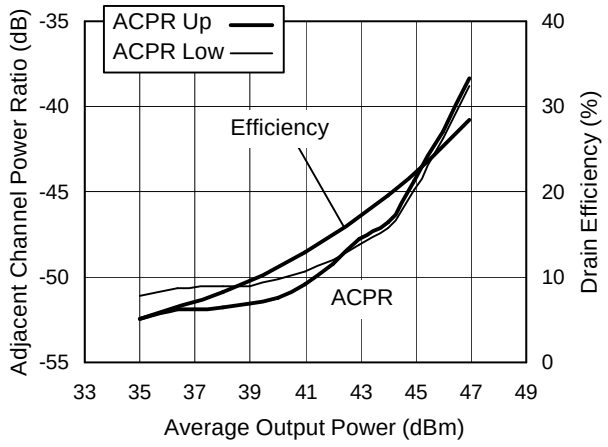
Power Sweep, CW Conditions

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 2170 MHz



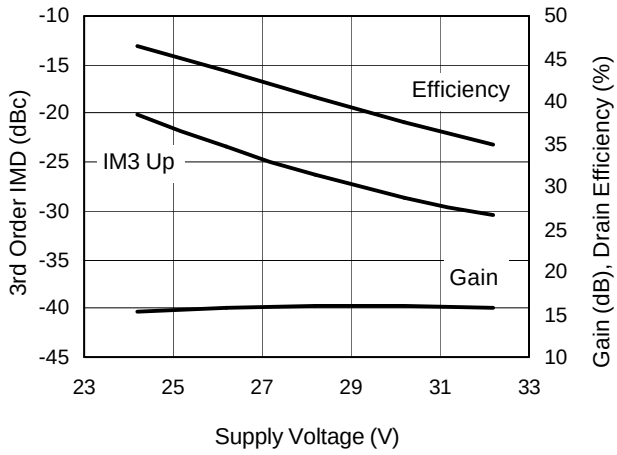
Single-carrier WCDMA Drive-up

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 2140 MHz,
3GPP WCDMA signal, TM1 w/16 DPCH, 67% clipping,
P/A R = 8.5 dB, 3.84 MHz BW



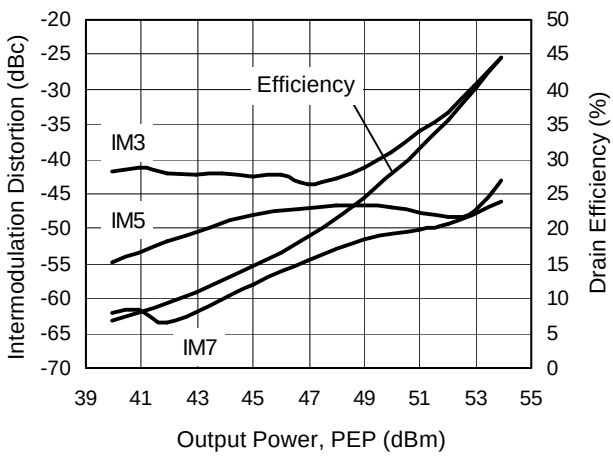
Voltage Sweep

I_{DQ} = 1600 mA, f = 2140 MHz,
tone spacing = 1 MHz, P_{OUT} (PEP) = 53 dBm



2-Tone Drive-up at Optimum I_{DQ}

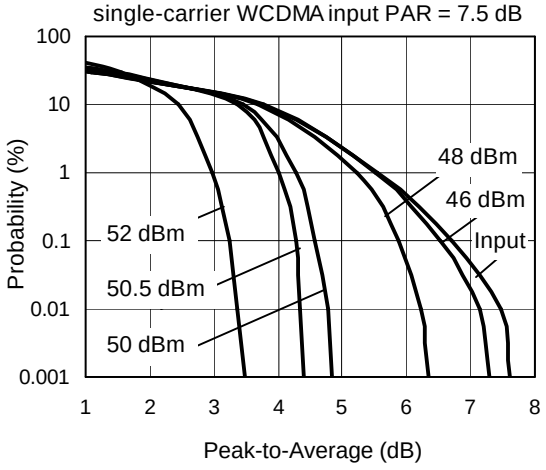
V_{DD} = 30 V, I_{DQ} = 1600 mA,
f = 2140 MHz, tone spacing = 1 MHz



Typical Performance (cont.)

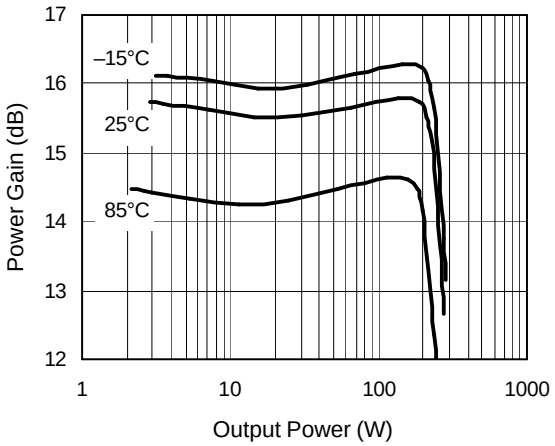
Output Peak-to-average Ratio Compression (PARC) at Various Power Levels

V_{DD} = 30 V, I_{DQ} = 1500 mA, f = 2170 MHz, single-carrier WCDMA input PAR = 7.5 dB



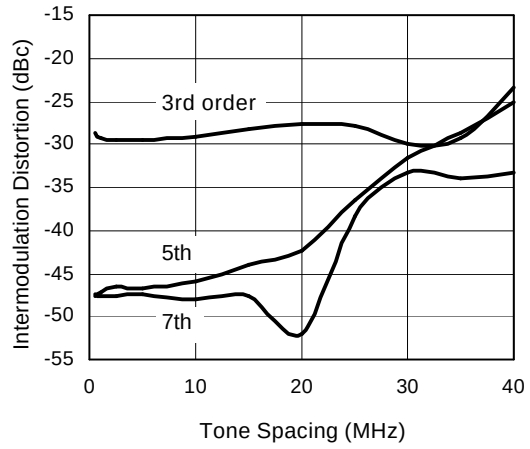
Power Gain vs. Power Sweep (CW) over Temperature

V_{DD} = 30 V, I_{DQ} = 1500 mA, f = 2170 MHz



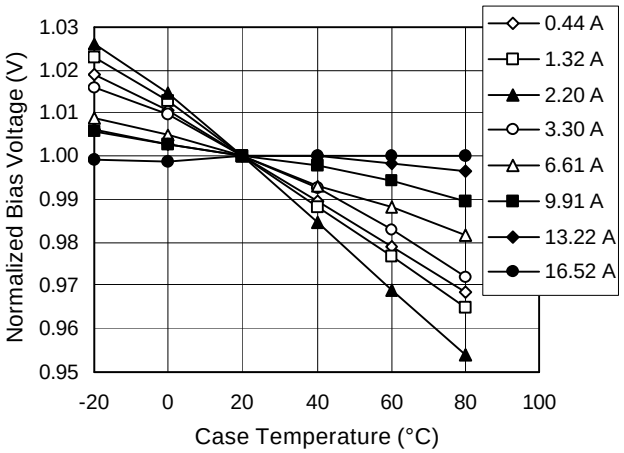
Intermodulation Distortion Products vs. Tone Spacing

V_{DD} = 30 V I_{DQ} = 1600 mA, f = 2140 MHz, P_{OUT} = 53 dBm PEP

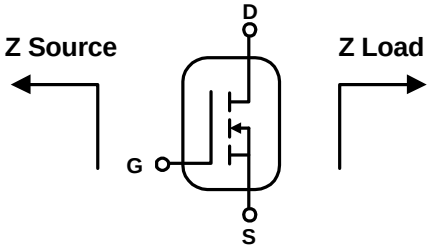


Bias Voltage vs. Temperature

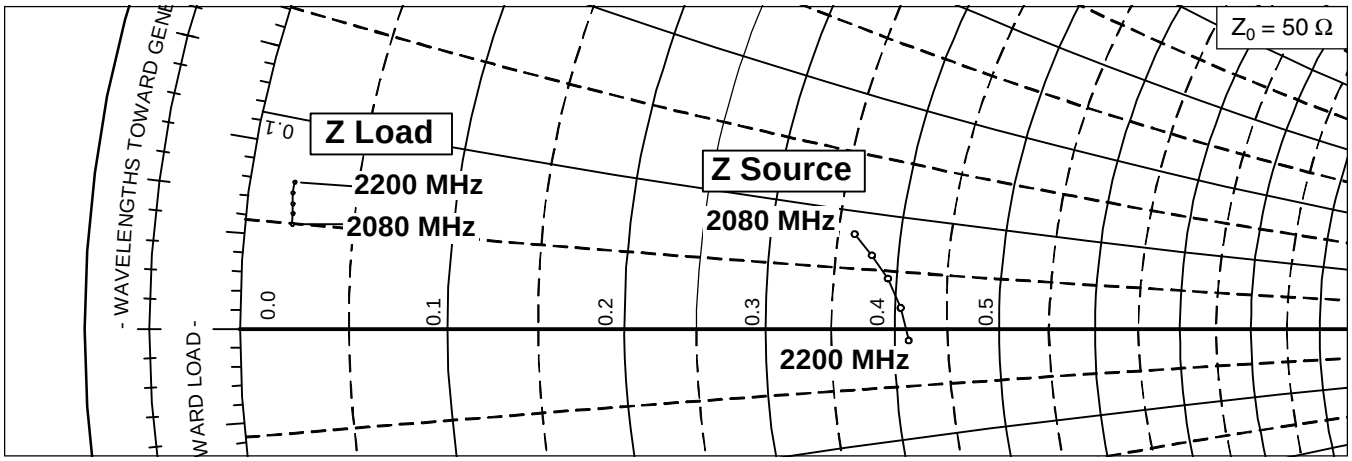
Voltage normalized to typical gate voltage, series show current



Broadband Circuit Impedance

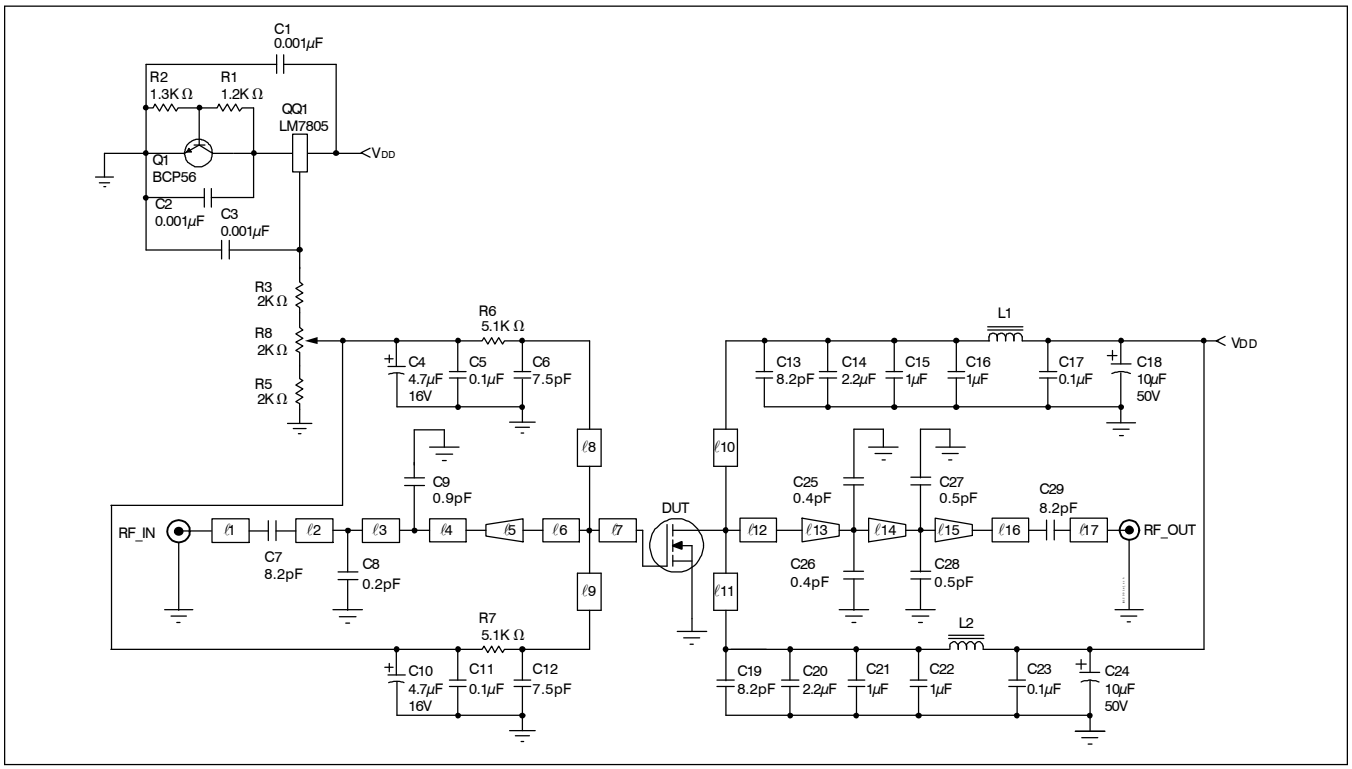


Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
2080	18.2	4.1	1.1	2.5
2110	19.0	3.2	1.0	2.8
2140	19.8	2.3	1.0	3.0
2170	20.4	1.0	1.0	3.2
2200	20.8	–0.6	1.0	3.5



See next page for circuit information

Reference Circuit



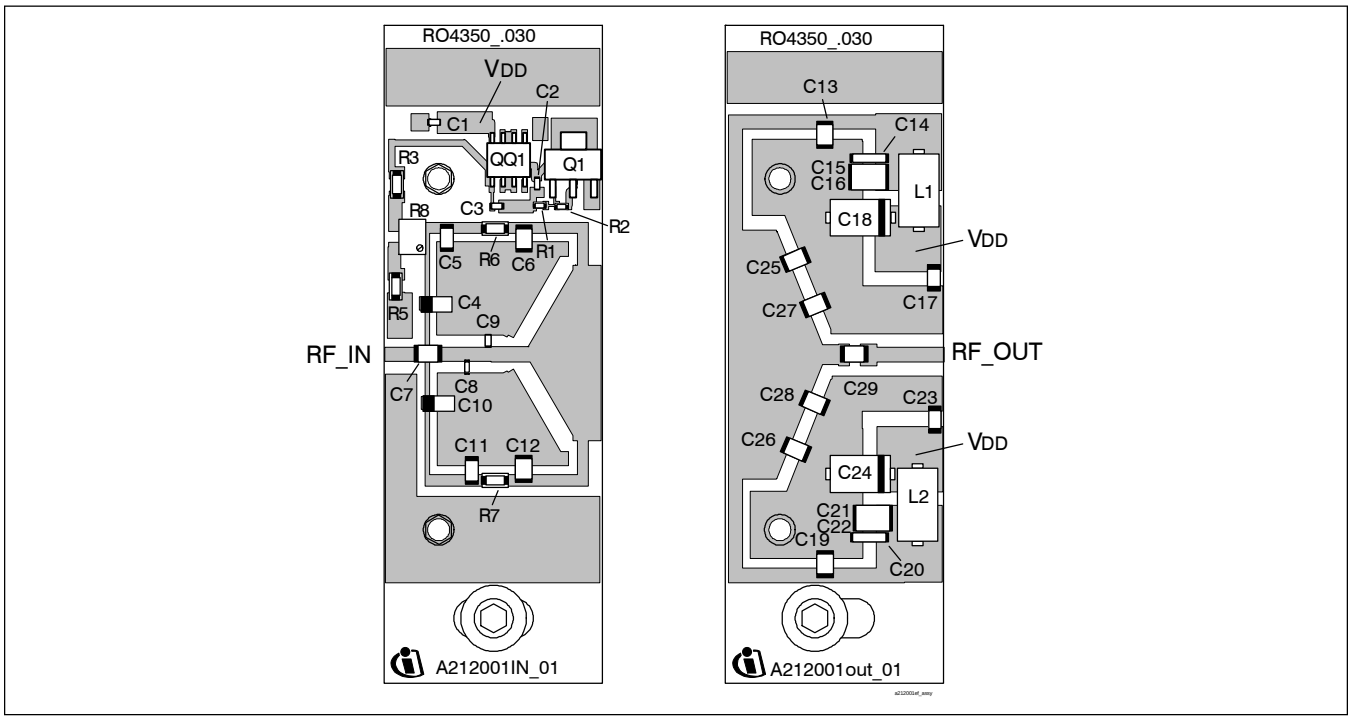
Reference circuit schematic for ƒ = 2140 MHz

Circuit Assembly Information			
DUT	PTFA212001E or PTFA212001F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 3.48	Rogers RO4350	1 oz. copper

Microstrip	Electrical Characteristics at 2140 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.042 λ, 50.0 Ω	3.56 x 1.68	0.140 x 0.066
ℓ2	0.048 λ, 50.0 Ω	4.11 x 1.68	0.162 x 0.066
ℓ3	0.026 λ, 50.0 Ω	2.08 x 1.68	0.082 x 0.066
ℓ4	0.059 λ, 50.0 Ω	5.03 x 1.68	0.198 x 0.066
ℓ5 (taper)	0.062 λ, 50.0 Ω / 6.9 Ω	5.00 x 1.68 / 20.32	0.197 x 0.066 / 0.800
ℓ6	0.015 λ, 6.9 Ω	1.14 x 20.32	0.045 x 0.800
ℓ7	0.028 λ, 6.9 Ω	2.16 x 20.32	0.085 x 0.800
ℓ8, ℓ9	0.136 λ, 60.0 Ω	11.63 x 1.27	0.458 x 0.050
ℓ10, ℓ11	0.254 λ, 51.2 Ω	21.51 x 1.65	0.847 x 0.065
ℓ12	0.071 λ, 5.0 Ω	5.49 x 28.83	0.216 x 1.135
ℓ13 (taper)	0.019 λ, 5.0 Ω / 6.8 Ω	1.52 x 28.83 / 20.62	0.060 x 1.135 / 0.812
ℓ14 (taper)	0.026 λ, 6.8 Ω / 13.5 Ω	2.11 x 20.62 / 9.65	0.083 x 0.812 / 0.380
ℓ15 (taper)	0.026 λ, 13.5 Ω / 40.9 Ω	2.06 x 9.65 / 2.34	0.081 x 0.380 / 0.092
ℓ16	0.029 λ, 40.9 Ω	2.77 x 2.34	0.109 x 0.092
ℓ17	0.107 λ, 50.0 Ω	9.04 x 1.68	0.356 x 0.066

[1]Electrical characteristics are rounded.

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4, C10	Capacitor, 4.7 µF, 16 V	Digi-Key	PCS3475CT-ND
C5, C11, C17, C23	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C12	Ceramic capacitor, 7.5 pF	ATC	100B 7R5
C7, C13, C19, C29	Ceramic capacitor, 8.2 pF	ATC	100B 8R2
C8	Ceramic capacitor, 0.2 pF	ATC	600S 0R2 BT
C9	Ceramic capacitor, 0.9 pF	ATC	600A 0R9 BT
C14, C20	Capacitor, 2.2 µF	Digi-Key	445-1474-2-ND
C15, C16, C21, C22	Ceramic capacitor, 1 µF	Digi-Key	445-1411-2-ND
C18, C24	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPSE106K050R0400
C25, C26	Ceramic capacitor, 0.4 pF	ATC	100B 0R4
C27, C28	Ceramic capacitor, 0.5 pF	ATC	100B 0R5
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infinion Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3, R5	Chip resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	not used		
R6, R7	Chip resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND
R8	Potentiometer 2 k-ohms	Digi-Key	3224W-202ETR-ND

** Gerber Files for this circuit available on request*

Package Outline Specifications

Package H-36260-2

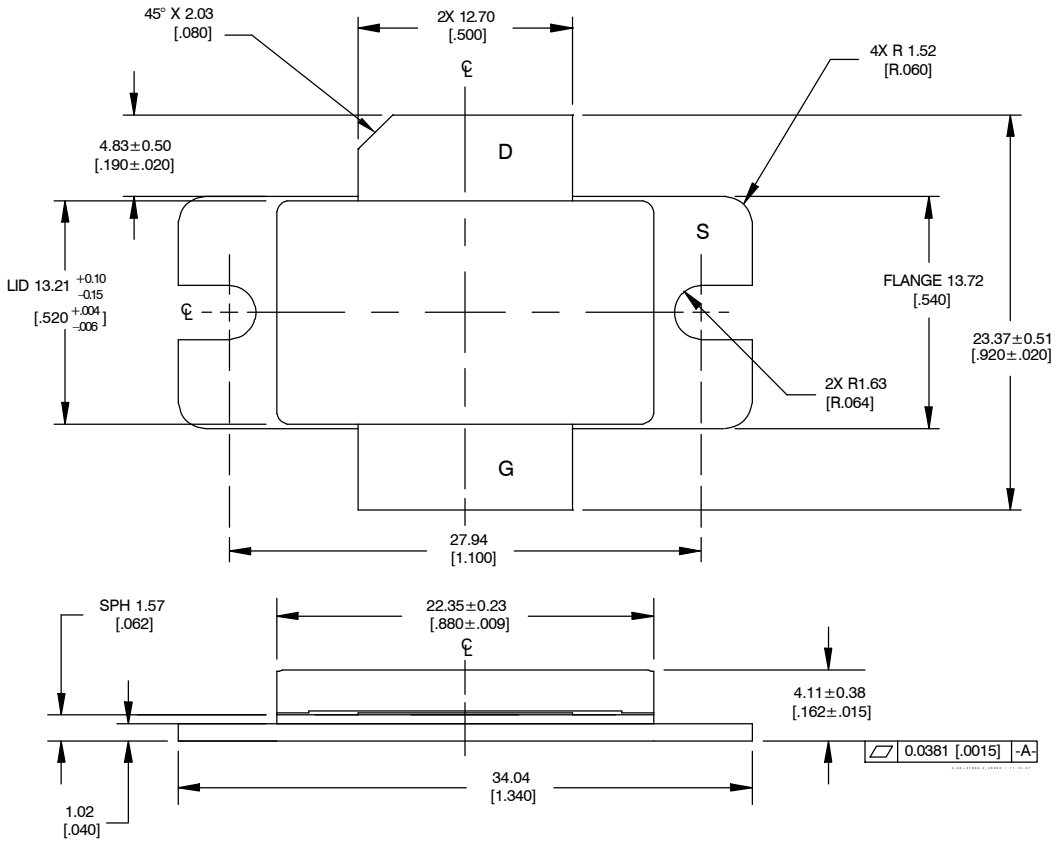


Diagram Notes—unless otherwise specified:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S, D, G - flange & leads: 1.14 ± 0.38 micron [45 ± 15 microinch]

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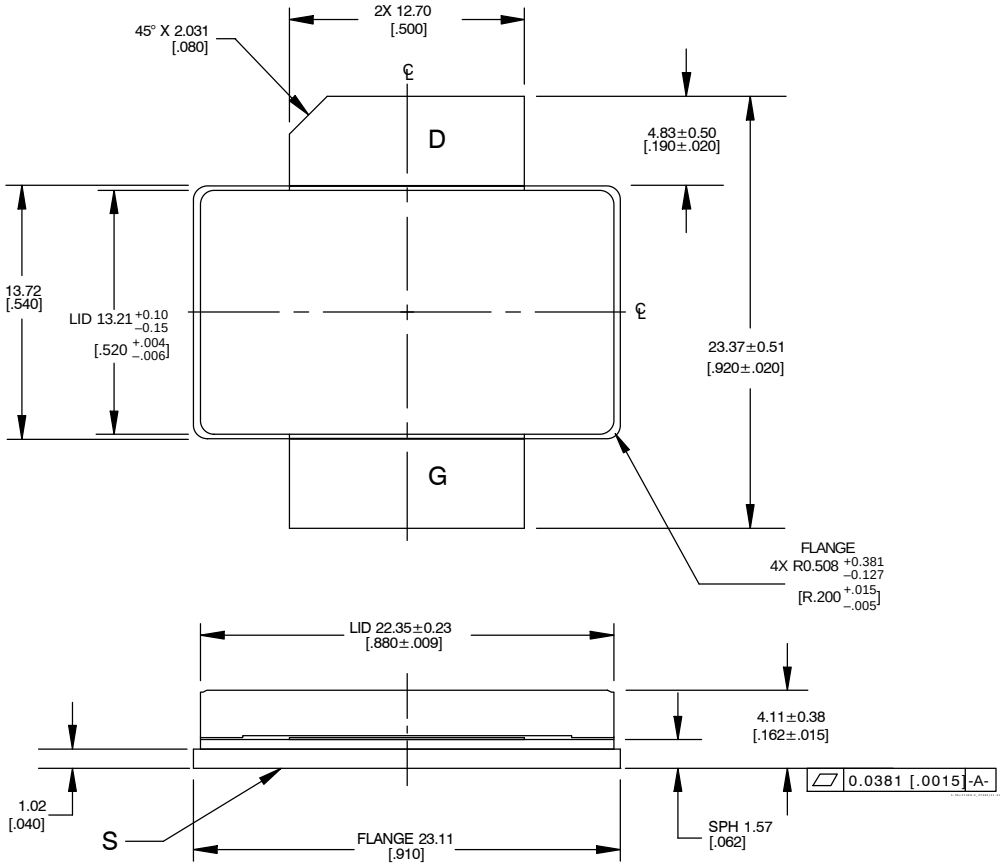
Package Outline Specifications (cont.)

Package H-37260-2



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Revision History:	2008-04-09	Data Sheet
Previous Version:	2007-12-05, Data Sheet (2006-06-12, Preliminary Data Sheet)	

Page	**Subjects (major changes since last revision)**
1, 2, 9, 10	Update product to V4, with new package technologies. Update package outline diagrams.
1, 2	Update gain specifications.

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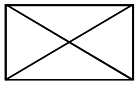

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